## REMARKS

The Office Action dated may 13, 2008 has been received and carefully noted. The following remarks are submitted as a full and complete response thereto.

Claims 1-60 are currently pending in the application, of which claims 1, 8, 13, 28, 32, 52, and 57 are independent. Applicants here amend claims 1, 2, 8-10, 13, 17, 18, 28, 32, 34, 36, 37, 52, and 57 to more distinctly claim the subject matter that the Applicants regard as the invention. Entry of the claim amendments is therefore respectfully requested because the amendments add no new subject matter to the present application and serve only to place the present application in better condition for allowance. All grounds for rejection in the Office Action are currently addressed, and the Applicants respectfully submit that the present application is in condition for allowance in view of the amendments and the following remarks. Reconsideration of claims 1-60 are respectfully requested.

Rejection under 35 U.S.C. 112, Second Paragraph

The Office Action rejected claims 1, 8, 13, 28, 32, 52, and 57 under 35 U.S.C. §112, second paragraph because the limitation of a "location" in the address resolution table was allegedly unclear. While Applicants respectfully disagree with this assertion because a person over ordinary skill in the field of networking would readily understand the meaning of a "location" in a table in a memory structure, Applicants here amended

this claims to clarify that a location within the address resolution table is configured to store a destination address associated with a packet.

The Office Action further alleged the limitation of a memory block in claim 34 lacked proper antecedent basis. Applicants here amend claim 34 to address this concern.

Applicants respectfully urge that this basis for rejection of claims 1, 8, 13, 28, 32, 34, 52, and 57 is now moot in view of these amendments and should be withdrawn. Reconsideration and allowance of claims 1, 8, 13, 28, 32, 34, 52, and 57 are therefore respectfully requested.

Rejection under 35 U.S.C. 103(a)

The Office Action rejected claims 1-6, 8-11, 13-15, 18-21, 23-25, 28-30, 32-34, 37-40, 42-44, 47-50, 52-55, and 57-60 under 35 U.S.C. 103(a) as being obvious over U.S. Patent No. 5,386,413 (McAuley) in view of U.S. Patent No. 6,279,097 (Kaku) and U.S. Patent No. 6,021,132 (Muller). Specifically, the Office Action took the position that McAuley disclosed all of the limitations of the independent claims except that a key is predefined portion of a packet destination address and that the sing buffer per packet mechanism, but that these deficiencies are cured, respectively by Kaku and Muller. Applicants submit that the cited references taken individually or in combination, fail to disclose or suggest all of the features of any of the pending claims.

Claim 1, from which claims 2-7 depend, recites a memory structure with an address resolution table. The address resolution table comprising a plurality of locations,

and each of the locations is configured to store a packet destination address. The address resolution table is configured to resolve addresses in a packet-based network switch and use a key to index one of the locations. The key is a predefined portion of the packet destination address associated with the location. The memory structure further includes a packet storage table configured to receive a packet for storage in the packet-based network switch and share a preselected portion of memory with the address resolution table. The memory structure further includes a single buffer per packet mechanism configured to receive an individual packet. The single buffer per packet mechanism is configured to perform only one transmit descriptor read per the individual packet and execute a single access in order to locate the packet and the packet destination address at the location using the key, whereby the entire packet is to be transmitted.

Claim 8, upon which claims 9-12 are dependent, recites a memory structure. The memory structure includes an address resolution table comprising an associative memory structure and uses a key to index a buffer within the address resolution table. The address resolution table comprising a plurality of locations, and each of the locations is configured to store a packet destination address. The address resolution table is configured to resolve addresses in a packet-based network switch and use a key to index one of the locations. The key is a predefined portion of the packet destination address associated with the location. The memory structure further includes a single buffer per packet mechanism configured to receive an individual packet. The single buffer per packet mechanism is configured to perform only one transmit descriptor read per the

individual packet and execute a single access in order to locate the packet destination address at the location using the key, whereby the entire packet is to be transmitted.

Claim 13, upon which claims 14-27 are dependent, recites a memory structure comprising a memory block. The memory structure includes an address resolution table comprising an associative memory structure. The address resolution table comprising a plurality of locations, and each of the locations is configured to store a packet destination address. The address resolution table is configured to resolve addresses in a packet-based network switch and use a key to index one of the locations. The key is a predefined portion of the packet destination address associated with the location. A transmit descriptor table is associated with a corresponding packet-based network transmit port, and the transmit descriptor table is configured to receive a table descriptor address and a table descriptor value. The packet storage table is configured to receive at least one of each of a packet data address portion and a packet data value portion. The memory structure further includes a single buffer per packet mechanism configured to receive an individual packet. The single buffer per packet mechanism is configured to perform only one transmit descriptor read per the individual packet and execute a single access in order to locate the packet destination address at the location using the key, whereby the entire packet is to be transmitted.

Claim 28, upon which claims 29-31 are dependent, recites a packet-based switch. The packet-based switch includes a shared memory structure comprising an address resolution table and a packet storage table. The address resolution table comprising a

plurality of locations, and each of the locations is configured to store a packet destination address. The address resolution table is configured to resolve addresses in a packet-based network switch and use a key to index one of the locations. The key is a predefined portion of the packet destination address associated with the location. The switch further includes a single buffer per packet mechanism configured to receive an individual packet. The single buffer per packet mechanism is configured to perform only one transmit descriptor read per the individual packet and execute a single access in order to locate the packet destination address at the location using the key, whereby the entire packet is to be transmitted.

Claim 32, upon which claims 33-51 are dependent, recites a packet-based switch comprising a memory structure. The memory structure includes an address resolution table comprising an associative memory structure. The address resolution table comprising a plurality of locations, and each of the locations is configured to store a packet destination address. The address resolution table is configured to resolve addresses in a packet-based network switch and use a key to index one of the locations. The key is a predefined portion of the packet destination address associated with the location. The memory structure includes a transmit descriptor table, the transmit descriptor table being associated with a corresponding packet-based network transmit port, and the transmit descriptor table configured to receive a table descriptor address and a table descriptor value. The memory structure includes a packet storage table, the packet storage table configured to receive at least one of each of a packet data address portion

and a packet data value portion. The switch further includes a single buffer per packet mechanism configured to receive an individual packet. The single buffer per packet mechanism is configured to perform only one transmit descriptor read per the individual packet and execute a single access in order to locate the packet destination address at the location using the key, whereby the entire packet is to be transmitted.

Claim 52, upon which claims 53-56 are dependent, recites a packet-based switch. The packet-based switch includes an address resolution table comprising a one-way associative memory structure. The address resolution table comprising a plurality of locations, and each of the locations is configured to store a packet destination address. The address resolution table is configured to resolve addresses in a packet-based network switch and use a key to index one of the locations. The key is a predefined portion of the packet destination address associated with the location. A packet data buffer table shares a memory block with an address resolution table. The switch further includes a single buffer per packet mechanism configured to receive an individual packet. The single buffer per packet mechanism is configured to perform only one transmit descriptor read per the individual packet and execute a single access in order to locate the packet destination address at the location using the key, whereby the entire packet is to be transmitted.

Claim 57, upon which claims 58-60 are dependent, recites a packet-based switch. The packet-based switch includes an address resolution table comprising a direct-mapped/one-way associative memory structure. The address resolution table comprising

a plurality of locations, and each of the locations is configured to store a packet destination address. The address resolution table is configured to resolve addresses in a packet-based network switch and use a key to index one of the locations. The key is a predefined portion of the packet destination address associated with the location. The switch further includes a single buffer per packet mechanism configured to receive an individual packet. The single buffer per packet mechanism is configured to perform only one transmit descriptor read per the individual packet and execute a single access in order to locate the packet destination address at the location using the key, whereby the entire packet is to be transmitted.

Applicants respectfully submit that each of the above claims recites features that are neither disclosed nor suggested in the cited references.

As described above, certain embodiments of the present invention relate to enabling a memory structure to resolve addresses in a packet-based network switch to enable bandwidth savings from a one buffer-per-packet approach. The single buffer-per-packet approach enhances the feasibility of a bit-per-buffer pool tracking technique and the need to search a larger buffer structure can be mitigated or eliminated. Thus, a packet-based switch performs one memory read for address resolution, and one memory write for address learning, to the address table for each frame received. Overhead is reduced and a reduction in accesses per frame is achieved. The single access for both read and write can be attributed to the single-entry direct-mapped address table.

In contrast, McAuley generally relates to a switch memory 100 for implementing a multilevel hierarchical routing table in a switch is disclosed. The switch memory 100 includes a plurality of mask circuits 120, 121 and 122, which each correspond to one level of the multilevel hierarchy. Each mask circuit 120, 121 and 122 receives a destination address of an incoming call or packet and masks out portions of the received destination address which do not correspond to the level of the hierarchy with which the mask circuit 120, 121 or 122 is associated. A memory array 130, 131 or 132 corresponding to each mask circuit 120, 121 or 122, is provided which is capable of storing a table of entries including an output port entry and a corresponding destination address of one level of the multilevel hierarchy of destination addresses. Additionally, each memory array 130, 131 or 132 may compare, in parallel, non-masked portions of the masked destination address outputted from the corresponding mask circuit 120, 121 or 122 with corresponding portions of each destination address of each table entry stored therein. Also, the switch memory 100 includes a prioritizer 150 for enabling the output of an output port entry of a matched table entry from the memory array 130, 131 or 132, storing destination addresses of the lowest level in the hierarchy, in which a match occurred.

Referring to claim 1, Applicants respectfully urge that McAuley fails to teach or suggest the limitation that the address resolution table is configured to use a key to index one of the locations. As described in the Office Action, McAuley reads the actual stored memory contents and compares the read contents with the destination address of the

packet to identify a corresponding stored network address in the memory. Thus, instead of resolving addresses, the cited CAMs 1-3 in McAuley are the stored addresses, with each of the CAMs storing a different portion of the address and being used to link with other address portions in the other CAMs to reform an entire address.

Moreover, McAuley discloses no "key" or other methodology for quickly identifying a pertinent memory location without examining the contents at that location. As described in the background section of the present application, conventional packet routing tools suffer from significant delays from searching for the destination addresses due to the need to read and analyze the memory contents, and McAuley does not teach or suggest the use of a key to address this problem.

Furthermore, as admitted in the Office Action, McAuley does not teach or suggest that limitation in claim 1 that the key is a predefined portion of the packet destination address associated with the location. As described above, McAuley discloses no key for searching for addresses. Moreover, as described above, McAuley discloses a hierarchical storage configuration in which portions of a destination address are stored across different tables. In this way, McAuley offers a different type of solution to finding an address by simplifying searches by searching smaller portions of the addresses. In contrast, embodiments of the present invention store and locate address data using the portions of the address data itself.

Continuing with claim 1, Applicants further note that the recited memory structure further includes a packet storage table that is configured to share a pre-selected portion of

memory with the address resolution table. As described above, McAuley does not disclose an address resolution table. Furthermore, even if it could be argued that one of the cited CAMs of McAuley serves and an address resolution table for another of the CAMs, there is no teaching or suggestion that the CAMs share a pre-selected portion memory. The portion from McAuley cited in the Office Action at col. 10, ll. 31-45 merely discloses that the size of memory can expanded as needed to store an entire address if needed (since, as described above, McAuley relates to storing and searching sub-portions of memory address).

Continuing with claim 1, Applicants further note that, as admitted in the Office Action, McAuley does not teach or suggest the limitation of a memory structure that includes a single buffer per packet mechanism configured to receive an individual packet, where the single buffer per packet mechanism is configured to perform only one transmit descriptor read per the individual packet and execute a single access in order to locate the packet destination address at the location using the key, where the entire packet is to be transmitted.

For at least these reasons, each of claims 1-60 is allowable over McAuley. As described in greater detail below, neither Kaku or Muller cure the these and other deficiencies in McAuley.

Kaku generally relates to a method of generating a lookup table includes receiving an input address, generating a compressed address from the input address, the compressed address comprising fewer bits than the input address, selecting a first set of

bits from the compressed address, determining whether a memory location pointed to by the first set of bits in an address lookup table includes an unoccupied memory slot, determining whether the input address matches any address stored in the memory location pointed to by the first set of bits in the address lookup table, and selecting a second set of bits from the compressed address in response to there not being an unoccupied memory slot in the memory location pointed to by the first set of bits and the input address not matching any address stored in the memory location pointed to by the first set of bits.

Specifically, a lookup table generator in Kaku includes an address compressor, a barrel shifter, and an address lookup table that includes a memory location that is pointed to by the first set of bits. A control state machine in Kaku is coupled to the barrel shifter and the address lookup table and is configured to shift the barrel shifter so that a second set of bits is selected from the compressed address in response to there not being an unoccupied memory slot in the memory location pointed to by the first set of bits and the input address not matching any address stored in the memory location pointed to by the first set of bits. Accordingly, the addressing system used in Kaku, although based upon the stored destination address, does not use key which "is a predefined portion of the packet destination address associated with the location." Instead, as described above, Kaku discloses a complex system in which a variety of methods and components by the location index can be defined, such that the index in Kaku is a dynamically created value

and not a "predefined" portion of the destination address contained at the indexed location.

Thus, contrary to the position taken in the Office Action, Kaku does not teach or suggest the limitation in claim 1 (and the other independent claims) of a key for a location of based upon the stored destination at that location. Moreover, Kaku is silent regarding a single buffer per packet mechanism configured to receive an individual packet, where the single buffer per packet mechanism is configured to perform only one transmit descriptor read per the individual packet and execute a single access in order to locate the packet destination address at the location using the key, where the entire packet is to be transmitted. For at least these reasons, Applicants urge that Kaku does not cure the above-described deficiencies in McAuley. Accordingly, the claims 1-60 are allowable over the combination of McAuley and Kaku.

Applicants further urge that McAuley and Kaku are technically incompatible and therefore, cannot be legally combined under 35 U.S.C. §103(a). As described above, McAuley discloses a routing system in which portions of the destination address are stored in a relational database, and that the address portions contained in the different tables within the relational database are acquired and compared to desired values. In other words, the data stored in the database in McAuley is compressed to minimize storage and checking requirements. In contrast, as described above, Kaku disclose complex rules for creating an index values for identifying memory locations storing complete address data, where the index for a location is created using the address data.

As discussed in Kaku, a key technical challenge in that reference is to preserve sufficient data in the index to allow the unique location of the stored address. In contrast, McAuley discusses opposite problem of storing minimum sufficient data to allow for the unique recreation of desired addresses from the relational database. Thus, following the implementation of the relational database in McAuley, no further compression of the stored data is possible for the creation of the index. Thus, there would be no technical motivation to combine McAuley and Kaku.

Moreover, as described above, McAuley relates to a relational database in which address data is stored across multiple tables. Applicants note that there is now easy way to apply Kaku to McAuley without undue experimentation, because Kaku does not relate to the technical problem of indexing multiple interlinked tables using compressed data contained within the tables. For these and other reasons, the combination of Kaku and McAuley is technically and legally improper. Therefore, claims 1-60 are further allowable over Kaku and McAuley on this separate legal basis.

Continuing with the Office Action, Muller does not cure these and other deficiencies in McAuley and Kaku.

Applicants again note that Muller is directed to shared memory management in a switch network element. Muller describes a shared memory manager 220 that is exploited by input and output ports 206 by locally storing pointers to buffers that contain packet data rather than locally storing the packet data. A predetermined number of buffer pointers are kept on hand to allow immediate storage of received packet data. The buffer

pointers are preallocated during the initialization of switching element 100 and requested from shared memory manager 220. Pointers are queued to buffers that contain packet data, and not to the packet data itself. Further, a packet can be stored over more than one buffer. Each buffer in shared memory 230 is owned by one or more different ports at different points in time without comprising to duplicate the packet data.

The Office Action takes the position that Muller discloses the single buffer per packet mechanism configured to receive an individual packet, as recited in claim 1. Specifically, the Office Action cited to Muller at FIG. 3A and stated that although Muller depicts the use of multiple buffers per packet, it would have been within the skill of ordinary skill in this technical field to adapt Muller for use as a single buffer. Applicants respectfully disagree with this finding. Specifically, Applicants note that Muller relates to dynamically providing a buffer such that only a correctly sized buffer is provided. As described in the background section of Muller at col. 2, ll. 1-10, incorrect buffer size leads to certain undesired inefficiencies.

Moreover, the Office Action does not address the limitation from claim 1 that the single buffer per packet mechanism is configured to perform "only one transmit descriptor read per the individual packet" and execute a single access in order to locate the packet destination address at the location using the key, wherein the entire packet is to be transmitted. Neither of these limitations is suggested or taught in Muller. Thus, the Office Action has not presented a legally sufficient rejection under 35 U.S.C. §103(a) and while claims of the present application have been amended for purposes of clarifying the

subject matter that the Applicants regard as the invention, as described above, any subsequent action must be non final because any subsequent rejection, if any, would not be necessitated by the present amendments (See MPEP §706.07(a)). Specifically, since this rejection is *de facto* legally and technically improper since the Office Action fails to address each and every limitation, any subsequent actions would necessarily introduces "a new ground of rejection that is neither necessitated by Applicants' amendment of the claims, nor based on information submitted in an information disclosure statement filed during the period set forth in 37 CFR §1.97(c) with the fee set forth in 37 CFR 1.17(p)."

Applicants respectfully submit that, as described above, the cited references of McAuley, Kaku, and Muller fail to disclose or suggest all of the features of the above claims for the reasons set forth above.

Applicants further urge that the combination of McAuley, Kaku, and Muller is legally improper under 35 U.S.C. §103(a). To establish *prima facie* obviousness the prior art references must teach or suggest all the claim limitations. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). As discussed above, the Office Action failed to establish prima facie obviousness because they cited references fail to disclose or suggest all of the features recited in any of the pending claims. Furthermore, as described above, Kaku and McAuley are technically incompatible and cannot be combined without undue experimentation. Applicants further note that no motivation is provided to combine Muller with either Kaku or McAuley, and that the Office Action has failed to provide a

*prima facie* rejection under 35 U.S.C. §103(a) for at least this reasons (see MPEP §§2141, 2143).

Still further, it is well established in U.S. Patent law that a piecemeal analysis of a number of references, to extract a number of individual elements which are picked and chosen in a mosaic to recreate the claimed invention, is improper absent some teaching or suggestion in the references to support their use in the particular claimed combination. It is improper to use applicant's own disclosure for any such motivation or incentive. Interconnect Planning Corporation v. Feil, 227 USPQ 543 (Fed. Cir. 1985), Symbol Technologies Inc. v. Opticon, Inc., 19 USPQ 1241 (Fed. Cir. 1991), In re Rothermel and Waddell, 125 USPQ 328 (CCPA 1960), In re Jones, 21 USPQ 2d 1941 (Fed. Cir. 1992).

In the present case, Applicants submit that the Office Action applies Muller and Kaku to cure the admitted deficiencies of McAuley. However, both Muller and Kaku are combined with McAuley in a piecemeal manner to recreate the features recited in the presently pending claims. For example, Kaku is combined with Muller and McAuley to add the feature that the key is a predefined portion of a packet destination address, and Muller is combined with McAuley and Kaku to add the feature of a one packet per buffer mechanism. One skilled in the art would not otherwise be motivated to combine McAuley, Kaku, and Muller except for the benefit of recreating Applicant's invention. Further neither McAuley, Kaku, nor Muller contain any motivation to do so. Thus, Applicants respectfully submit that portions of Kaku, and Muller were extracted in an effort to recreate the features recited in the pending claims.

Applicants respectfully submit that because claims 2-7, 9-12, 14-27, 29-31, 33, 51, 53-56 and 58-60 depend from claims 1, 8, 13, 28, 32, 52 and 57, these claims are allowable at least for the same reasons as claims 1, 8, 13, 28, 32, 52 and 57, as well as for the additional features recited in these dependent claims.

Based at least on the above, Applicants respectfully submit that McAuley, Kaku, and Muller, taken individually or in combination, fail to disclose or suggest all of the features recited in claims 1-6, 8-11, 13-15, 18-21, 23-25, 28-30, 32-34, 37-40, 42-44, 47-50, 52-55, and 57-60. Accordingly, withdrawal of the rejection under 35 U.S.C. §103(a) is respectfully requested.

The Office Action rejected claims 7, 12, 22, 31, 41, 51, and 56 under 35 U.S.C. §103(a) as being obvious over McAuley, in view of Kaku and Muller, further in view of U.S. Patent No. 5,765,036 (Lim) . Specifically, the Office Action took the position that McAuley, Kaku, and Muller disclosed all of the features of the independent claims 1, 8, 13, 23, 32, and 52, as described above, and Lim disclosed the additional limitation in these claims. Applicants submit that the cited references taken individually or in combination, fail to disclose or suggest all of the features of any of the pending claims.

Lim discloses a shared memory system (10) which includes interfaces with a shared memory bus (14). The shared memory bus (14) in Lim interfaces with a plurality of peripherals (12) through memory interfaces (16). Each of the memory interfaces (16) is operable to receive addresses from the associated one of the peripheral units (12) and

communicate with the shared memory system (10) to process the addresses and subsequent data transfers in an ordered manner. The shared memory system (10) in Lim further is associated with an arbitration logic circuit (78) that is operable to service bus requests from each of the memory interfaces (16). When a bus request is received in Lim, a requesting memory interfaces (16) is allowed to access a single byte of data, after which it relinquishes the bus to another one of the memory interfaces (16). The previous buses that performed the one byte data transfer operation is then lowered in its priority such that all the memory interfaces (16) may transfer at least one byte of data. This memory access configuration results in a byte-by-byte transfer of data without allowing any one of the memory interfaces (16) to seize and hold the bus for multiple data transfers in a sequential manner.

In another mode, each of the memory interfaces (16) in Lim may seize the bus to continuously transfer data with a priority system implemented to allow a higher priority one to seize the bus away from the lower priority one. Thus, Lim discloses that a memory access "cycle" may be modified to allow necessary operations to occur within a cycle. For example, as described above, multiple memory accesses may be performed within that dynamically defined cycle. In contrast, embodiments of the present invention relate to providing a configuration in which necessary data location and access operation may be performed within a single computation "cycle," where as Lim relates to defining a single memory cycle that can take multiple processing cycles, such making multiple

memory locations. Thus, Lim fails to teach or suggest the limitation in claim 7, 12, and 31.

Moreover, as described above, McAuley, Kaku, and Muller fail to disclose each and every limitation of claims 1, 8, 13, 28, 32, 52 and 57. Lim fails to cure these deficiencies. Referring to claim 1, for example, Applicants note that Lim does not teach or suggest recited limitations of an address resolution table, a packet storage table, and a single buffer per packet mechanism. Thus, claim 1 is allowable over the combination of McAuley, Kaku, Muller, and Lim. Likewise, each of claim 8, 13, 28, 32, 52 and 57, although patentably distinct, is similarly allowable over McAuley, Kaku, Muller, and Lim on a similar basis. Dependent claims 7, 12, 22, 31, 41, 51, and 56 are therefore also allowable over McAuley, Kaku, Muller, and Lim, as well as for the separate limitations recited in these claims.

Continuing with the Office Action. claims 16, 17, 35, and 36 are rejected under 35 U.S.C. 103(a) as being obvious over McAuley, in view of Kaku and Muller, further in view of U.S. Patent No. 6,279,097 (Liu). Specifically, the Office Action took the position that McAuley, Kaku, and Muller disclosed all of the features of the independent claims, as described above, and Liu disclosed the additional limitation in claims 16, 17, 35, and 36 of a FIFO memory structure. Applicants submit that the cited references taken individually or in combination, fail to disclose or suggest all of the features of any of the pending claims.

Liu relates to a method of generating a lookup table that includes receiving an input address, generating a compressed address from the input address, the compressed address having fewer bits than the input address, selecting a first set of bits from the compressed address, determining whether a memory location pointed to by the first set of bits in an address lookup table includes an unoccupied memory slot, determining whether the input address matches any address stored in the memory location pointed to by the first set of bits in the address lookup table, and selecting a second set of bits from the compressed address in response to there not being an unoccupied memory slot in the memory location pointed to by the first set of bits and the input address not matching any address stored in the memory location pointed to by the first set of bits.

For example, a lookup table generator in Liu includes an address compressor, a barrel shifter, and an address lookup table that includes a memory location that is pointed to by the first set of bits. A control state machine is coupled to the barrel shifter and the address lookup table and is configured to shift the barrel shifter so that a second set of bits is selected from the compressed address in response to there not being an unoccupied memory slot in the memory location pointed to by the first set of bits and the input address not matching any address stored in the memory location pointed to by the first set of bits.

Moreover, as described above, McAuley, Kaku, and Muller fail to disclose each and every limitation of claims 1, 8, 13, 28, 32, 52 and 57. Liu fails to cure these deficiencies. Referring to claim 1, for example, Applicants note that Liu also does not

teach or suggest recited limitations of an address resolution table, a packet storage table, and a single buffer per packet mechanism. Thus, claim 1 is allowable over the combination of McAuley, Kaku, Muller, and Liu. Likewise, each of claim 8, 13, 28, 32, 52 and 57, although patentably distinct, is similarly allowable over McAuley, Kaku, Muller, and Liu on a similar basis. Dependent claims 16, 17, 35, and 36 are therefore also allowable over McAuley, Kaku, Muller, and Liu, as well as for the separate limitations recited in these claims.

The Office Action further rejected claims 26, 27, 45, and 46 under 35 U.S.C. 103(a) as being obvious over McAuley, in view of Kaku and Muller, further in view of U.S. Patent No. 5,940,375 (Soumiya). Specifically, the Office Action took the position that McAuley, Kaku, and Muller disclosed all of the features of the independent claims, as described above, and Soumiya disclosed the additional limitation in these claims of a LIFO memory Applicants submit that the cited references taken individually or in combination, fail to disclose or suggest all of the features of any of the pending claims.

Soumiya generally relates to a feedback control apparatus in which the control loop for available bit rate (ABR) connections is segmented into multiple loops that are mutually handled for better responsiveness of ABR connection feedback control. For example, three control may be formed: a closed upward feedback control loop between a source end system and a virtual destination-link unit (VD-L) for an ABR connection, a downward control loop between a destination end system and a virtual source-link unit

(VS-L) for the ABR connection, and an intra-switch feedback control loop between an upstream virtual source-internal unit (VS-I) and a downstream virtual destination-internal unit (VD-I) for the ABR connection.

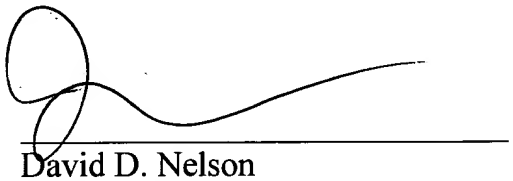
Moreover, as described above, McAuley, Kaku, and Muller fail to disclose each and every limitation of claims 1, 8, 13, 28, 32, 52 and 57. Soumiya fails to cure these deficiencies. Referring to claim 1, for example, Applicants note that Soumiya also does not teach or suggest recited limitations of an address resolution table, a packet storage table, and a single buffer per packet mechanism. Thus, claim 1 is allowable over the combination of McAuley, Kaku, Muller, and Soumiya . Likewise, each of claim 8, 13, 28, 32, 52 and 57, although patentably distinct, is similarly allowable over McAuley, Kaku, Muller, and Soumiya on a similar basis. Dependent claims 26, 27, 45, and 46 are therefore also allowable over McAuley, Kaku, Muller, and Soumiya, as well as for the separate limitations recited in these claims.

In view of the above comments, Applicants respectfully submit that each of claims 1-60 is in condition for allowance. Accordingly, Applicants respectfully request that each of claims 1-60 be allowed, and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicants' undersigned representative at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicants respectfully petition for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



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